

5973 U.S. PTO
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02/14/02

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PATENT NUMBER and
ISSUE DATE

U.S. UTILITY Patent Application

| APPL NUM | FILING DATE | CLASS | SUBCLASS | GAU | EXAMINER |
|---|-------------|---|----------|--------------------|--------------------|
| 10077258 | 02/14/2002 | 257 | 324 | 2814 | <i>[Signature]</i> |
| **APPLICANTS: Mo Brian; Chau Duc; <i>yft</i> | | | | | |
| **CONTINUING DATA VERIFIED: <i>yel</i> THIS APPLICATION IS A DIV OF 09/286,168 04/05/1999 <i>yft</i> | | | | | |
| BEST AVAILABLE COPY | | | | | |
| ** FOREIGN APPLICATIONS VERIFIED: <i>none yft</i> | | | | | |
| PG-PUB <input type="checkbox"/> DO NOT PUBLISH <input type="checkbox"/> | | RESCIND <input type="checkbox"/> | | | |
| Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no | | 35 USC 119 conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no | | ATTORNEY DOCKET NO | |
| Verified and Acknowledged Examiners's initials <i>yft</i> | | | | 018865-001010US | |
| TITLE : Method of forming a trench transistor having a superior gate dielectric U.S. DEPT. OF COMM./PAT. & TM.-PTO-4361 (Rev. 12-94) | | | | | |

| | | | |
|---|-----------|---------------------------|---------------------------|
| NOTICE OF ALLOWANCE MAILED | | CLAIMS ALLOWED | |
| | | Total Claims 10 | Print Claim for O.G. 1 |
| ISSUE FEE | | DRAWING | |
| Amount Due | Date Paid | Sheets Drwg. 5 | Figs. Drwg. 7 |
| | | Print Fig. 3, 4 | |
| <input type="checkbox"/> TERMINAL DISCLAIMER | | Primary Examiner | |
| | | PREPARED FOR ISSUE | |
| | | Application Examiner | |
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